REMARKS

The present Amendment is submitted with an RCE in accordance with 37 CFR §1.114. This Amendment is in response to the Final Office Action of July 25, 2002. Applicants note that a Proposed Amendment was submitted on September 24, 2002, and an Advisory Action issued from the Office on October 10, 2002. The Advisory Action stated that the Proposed Amendment would not be entered as raising new issues requiring further consideration and/or search, and not deemed to place the application in better form for appeal. In a subsequent telephone conference on October 21, 2002, between the Examiner and counsel for Applicants, the Examiner stated that, as submitted by counsel for Applicants, the Proposed Amendment did in fact remove issues on Appeal, if Appeal were to be taken. Specifically, Applicants' proposed amendment to claim 16 removed the §112 rejection of claims 16 and 18-21. However, no Supplemental or Corrected Advisory Action has been received by Applicants, and Applicants herein re-submit the proposed amendments as if they have not been previously entered.

Accordingly, Claims 14-21 stand rejected as described below. Claims 14-21 and 33-40 are pending after entry of this Amendment. Claims 14-21 are herein amended as described below, and new claims 33-40 are herein submitted for examination. Applicants respectfully submit that all amendments and new claims are fully supported in the specification as originally filed, and no new matter is claimed or introduced.

Rejections under 35 U.S.C. §112

Claims 16, and 18-21 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Specifically, the Office has maintained the §112 rejection based on the phrase "at least about" at line 3 of claim 16. Applicants herein amend line 3 of claim 16 to recite --at least--. Applicants therefore respectfully request that the §112 rejection be withdrawn.

Rejections under 35 U.S.C. §103

Claims 14-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Degner et al. (U.S. Patent No. 5,074,456) in view of Chang et al. (U.S. Patent No 4,854,263). This rejection is respectfully traversed.

Applicants' independent claim 14, as amended herein, claims a method for processing a semiconductor wafer through plasma etching operations. In a chamber for processing a semiconductor wafer through plasma etching operations, the chamber being in an operational state and including a support chuck for holding the semiconductor wafer, a pair of RF power sources, and a top electrode, the method for processing a semiconductor wafer through plasma etching operations includes striking a plasma in a plasma region of the chamber, and generating an increase in bias voltage directed at a wafer surface of the semiconductor wafer and a decrease in bias voltage directed at the top electrode. The top electrode is claimed as having a center region, a first surface and a second surface. The first surface has an inlet that is configured to receive processing gases from a source that is external to the chamber, and to flow the processing gases into the center region. The second surface has a plurality of gas feed holes that lead to a plurality of electrode openings. The plurality of electrode openings have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes. The plurality of electrode openings are configured to define the second surface which is located over the wafer surface of the semiconductor wafer. When a plasma is struck in the plasma region defined between the second surface and the wafer surface, the plasma defines a first plasma sheath surface that has a first plasma sheath surface area that is proximate to the wafer surface, and a second plasma sheath surface that has a second plasma sheath surface area that is proximate to the second surface. The second plasma sheath surface area is greater than the first plasma sheath surface area.

Applicants' new independent claim 33 claims a method of processing a semiconductor wafer. The method includes providing a processing chamber. The processing chamber is in an operational state and includes a top electrode, a wafer support chuck that has the semiconductor wafer positioned thereon, and a pair of RF power sources. The method then includes striking a plasma within a plasma region of the processing chamber, and causing a first surface of a plasma sheath to shift into electrode openings of the top electrode. The plasma sheath defines the first surface of the plasma sheath next to the top electrode and a second surface of the plasma sheath over a surface of the semiconductor wafer.

Applicants' new independent claim 37 claims a method for high aspect ratio semiconductor etching. The method includes providing a plasma etch processing chamber which includes a top electrode, a wafer support chuck, and a pair of RF power supplies, and is configured in an operational state. A plasma is struck in a plasma region

of the chamber. The plasma region is defined between an electrode surface of the top electrode and a wafer surface of a wafer which is positioned on the wafer support chuck. A first surface of a plasma sheath which is proximate to the top electrode is caused to shift into electrode openings of the top electrode. A bias voltage over the wafer surface is increased while the bias voltage over the electrode surface of the top electrode is decreased without increasing a plasma density.

Degner et al. show a composite electrode useful particularly in parallel plate plasma reactor apparatus. Degner et al. teach a pair of baffle plates located between a backing plate and an electrode plate, as well as a plurality of orifices in the electrode plate through which reactant gases are distributed. However, Degner et al. does not show or suggest the Applicants' electrode or claimed methods of implementation. According to Degner et al., "The [electrode] plate will generally be flat and free from protuberances..." Although Degner et al. do not describe in detail the reactant gas orifices, the design and purpose of the orifices is essentially for introduction of reactant gases while minimizing "non-uniformities in the thermal, electrical, and structural properties of the disk." Degner et al. shows a flat-surfaced, composite electrode. Such an electrode cannot result in causing the plasma sheath to shift.

Chang et al. describe a gas manifold that can act as an electrode used in a plasma-enhanced chemical vapor deposition system (PECVD). Essentially, Chang et al. teach chemical vapor deposition onto a substrate, and the stated objects are providing a gas manifold designed to increase the dissociation and reactivity of gases such as nitrogen, providing an improved parallel plate and gas inlet manifold configuration for forming low hydrogen content silicon nitride films at high deposition rates using nitrogen with reduced ammonia or without ammonia. Chang et al. also state that an objective of the invention is to provide an improved parallel plate electrode and gas inlet manifold configuration for forming silicon oxide films and for forming low hydrogen content silicon oxynitride films at high deposition rate using nitrogen with reduced ammonia or without ammonia. Chang et al. do not teach or suggest, at least, causing the plasma sheath to shift, increasing the bias voltage on the surface of the wafer without increasing plasma density, or increasing the ion bombardment.

Degner et al. and Chang et al., either standing alone or in combination, fail to teach or suggest Applicants' presently claimed invention. Applicants respectfully submit that independent claims 14, 33, and 37 are patentable over Degner et al., over Chang et al., and over Degner et al. in view of Chang et al. Claims 15-21, 34-36, and 38-40, each

of which directly or indirectly depends from one of independent claims 14, 33, and 36 are all likewise patentable for at least the same reasons.

In view of the foregoing, Applicants respectfully submit that claims 14-21 as amended, and new claims 33-40 are in condition for allowance. Accordingly, a Notice of Allowance is respectfully requested. If Examiner has any questions concerning the present amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6900, ext. 6905. If any additional fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. LAM1P077A).

Respectfully submitted,
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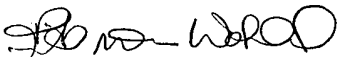

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MARKED UP CLAIMS:

The claims are herein amended as indicated.

14. (Three Times Amended) [A method for making a top electrode for use in] In a chamber for processing a semiconductor wafer through plasma etching operations, the chamber being in an operational state and including a support chuck for holding the semiconductor wafer, [and] a pair of RF power sources, and a top electrode, [the] a method for processing a semiconductor wafer through plasma etching operations, comprising:

striking a plasma in a plasma region of the chamber; and

generating an increase in bias voltage directed at a wafer surface of the semiconductor wafer and a decrease in bias voltage directed at the top electrode, [forming] the top electrode [to have] having a center region, a first surface and a second surface, the first surface [has] having an inlet that is configured to receive processing gases from a source that is external to the chamber and flow the processing gases into the center region, the second surface [has] having a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings [are] being configured to define the second surface which is located over [a] the wafer surface of the semiconductor wafer,

wherein when a plasma is struck in the plasma region defined between the second surface and the wafer surface, the plasma defines a first plasma sheath surface having a first plasma sheath surface area that is proximate to the wafer surface and a second plasma sheath surface having a second plasma sheath surface area that is proximate to the

second surface, the second plasma sheath surface area being greater than the first plasma sheath surface area.

15. (Amended) The method for [making a top electrode for use in the chamber] processing a semiconductor wafer through plasma etching operations as recited in claim 14, further comprising:

coupling the top electrode to one of the pair of RF power sources and the support chuck to the other one of the pair of RF power sources.

16. (Three Times Amended) The method for [making a top electrode for use in the chamber] processing a semiconductor wafer through plasma etching operations as recited in claim [15] 14, further comprising:

causing the second plasma sheath surface having the second plasma sheath surface area to shift into the electrode openings of the second surface of the top electrode, [forming] the electrode openings [to be] being at least [about] 0.5 mm or greater in diameter and the gas feed holes [to have] having a diameter of about 0.1 mm.

17. (Amended) The method for [making a top electrode for use in the chamber] processing a semiconductor wafer through plasma etching operations as recited in claim [15] 16, further comprising:

defining the electrode openings to a depth of between about 1/32 inch and ¼ inch.

18. (Amended) The method for [making a top electrode for use in the chamber] processing a semiconductor wafer through plasma etching operations as recited in claim 16, further comprising:

fixing a separation of between about 0.75 cm and about 4 cm between the [electrode] second surface and the wafer surface.

19. (Amended) The method for [making a top electrode for use in the chamber] processing a semiconductor wafer through plasma etching operations as recited in claim 18, further comprising:

inserting two or more gas buffer plates within the center region of the top electrode.

20. (Twice Amended) The method for [making a top electrode for use in the chamber] processing a semiconductor wafer through plasma etching operations as recited in claim 18, further comprising:

[striking a plasma between the separation, the plasma having a first plasma sheath surface area that is proximate to the wafer surface and a second plasma sheath surface area that outlines an inner region of the top electrode openings, such that the second plasma sheath surface area is greater than the first plasma sheath surface area]

fixing a separation between the second plasma sheath surface having the second plasma sheath surface area and the second surface of the top electrode at between about 0.5 mm and about 5 mm.

21. (Amended) The method for [making a top electrode for use in the chamber] processing a semiconductor wafer through plasma etching operations as recited in claim [20] 14, further comprising:

increasing an ion bombardment energy over the wafer surface when the second plasma sheath surface area is greater than the first plasma sheath surface area.